AN ELECTRONIC SWITCHING DEVICE FOR A UNIVERSAL SERIAL BUS INTERFACE

FIELD OF THE INVENTION

The present invention relates to a switching device for a universal serial bus interface, and more particularly to an electronic switching device that can connect a plurality of device each having a universal serial bus interface, so as to share related resources.

BACKGROUND OF THE INVENTION

All of the conventional switching devices for a universal serial bus (USB) interface are mechanical switching devices. The switching action of the mechanical switching device is a kind of sequential switching, therefore, when the switch passes the intermediate unrelated connection points, the related electronic signal will cause unrelated devices to operate, even though the connection time is very short. When the switching between related devices is very fast, the related devices may not operate accurately.

Furthermore, a mechanical switching device is apt to form the disconnection problem, and sometimes is not very easy to twist/turn.

OBJECTS OF THE INVENTION

It is therefore an object of the present invention to provide an electronic switching device for a universal serial bus interface, such that when enabling the switch sequentially to select a related device, due to a delay signal generator design the intermediate devices will not operate.

2

It is another object of the present invention to provide an electronic switching device for a universal serial bus interface, so as to replace the conventional mechanical switching device to avoid the disconnection problem, and the twist/turn problem.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be better understood with the following drawings, in which:

Fig. 1 is a schematic block diagram according to a first embodiment of the present invention.

Figs. 2 is the circuit diagram of the first embodiment of the present invention.

Fig. 3 is the circuit diagram of a second embodiment according to the present invention.

Fig. 4 is the circuit diagram of a third embodiment according to the present invention.

Fig. 5 is a schematic block diagram of the first embodiment of the present invention showing that a delay signal generator is added.

Fig. 6 is a schematic circuit diagram of the first embodiment of the present invention showing that a delay signal generator is added.

Fig. 7 is a schematic block diagram of the first embodiment of the present invention showing that a display is added.

Fig. 8 is a schematic circuit diagram of the first embodiment of the present invention showing that a display is added.

Fig. 9 is a schematic block diagram of the first embodiment of the present invention showing that an enable signal generator is added.

Fig. 10 is a schematic circuit diagram of the first embodiment of the present invention showing that an enable signal generator is added.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Fig. 1, which is a schematic block diagram according to a first embodiment of the present invention. As shown in the figure, a trigger signal generator 11, a control signal generator 12, and a connector 13 are included, in which:

the trigger signal generator 11 having an output to be connected with an input of the control signal generator 12, and having a switch SW1 (please see Fig. 2) to output a trigger signal to control signal generator 12 when a user pushes the switch SW1 down;

the control signal generator 12 having an input to be connected with an output of the trigger signal generator 11, and having an ouput to be connected with an input of the connector 13, for receiving the trigger signal outputted from the trigger signal generator 11, and processing the trigger signal, then outputting a control signal to the connector 13;

the connector 13 having an input to be connected with a first universal serial bus (USB) interface 14 and a second universal serial bus (USB) interface 15, and having an output to be connected with a third universal serial bus (USB) interface 16. When the connector 13 receives the control signal outputted from the the control signal generator 12, the connector 13 will connect the third USB interface 16 with the first USB interface 14 or the second USB interface 15.

Next referring to Fig. 2, a detailed circuit of the first

embodiment according to the present invention will be described. A trigger signal generator 11, a control signal generator 12, and a connector 13 are included, in which:

the trigger signal generator 11 comprising a resistor R1, a capacitor C1, and a switch SW1. The resistor R1 and the capacitor C1 are serially connected between VCC and ground (GND). One end of the resistor R1 is connected with VCC, the other end of the resistor R1 is connected with one end of the capacitor C1, the other end of the capacitor C1 is connected with GND. One end of the switch SW1 is connected to GND, the other end of the switch SW1 is connected to where the resistor R1 is connected with the capacitor C1, having a voltage V1. Before the switch SW1 is enabled, the switch SW1 does not conduct, and voltage V1 will be maintained at a HIGH voltage; when the switch SW1 is enabled, it will conduct, voltage V1 will be connected to GND, so as to change the HIGH voltage to LOW voltage. When SW1 is opened again, voltage V1 will return to HIGH voltage due to the charging of the capacitor C1. Therefore, open/short actions of SW1 will cause the capacitor C1 charging/discharging, and make the voltage V1 HIGH/LOW so as to generate a pulse signal to be used as a trigger signal to control the control signal generator 12;

the control signal generator 12 comprising a first D FLIP-FLOP (or an equivalent circuit) U2. The clock signal input terminal CP of the first D FLIP-FLOP U2 is connected with the output of the trigger signal generator 11, while the reverse data output terminal QN is connected with the data input terminal D, and the output signal from the positive data output terminal Q is used as the control signal

5

of the connector 13. When the clock signal input terminal CP receives a pulse signal, the voltage of terminal D will be moved to terminal Q, while a reverse voltage of the original voltage of the termunal D will be formed at terminal QN, and the voltage of the terminal QN will then be sent back to terminal D. When the terminal CP receives the next pulse signal, the first D FLIP-FLOP U2 will repeat the above procedures. Therefore, when the terminal CP receives pulse signals continuously, the HIGH voltage and the LOW voltage will be outputted alternately, and used as the control signals for the connector 13;

the connector 13 comprising a first multiplexor U3 (or an equivalent circuit), the first set of signal input terminal X1 and Y1 is connected with the first USB interface 14, the second set of signal input terminal X2 and Y2 is connected with the second USB interface 15, the third set of signal input terminal X3 and Y3 is connected with the third USB interface 16, while a selecting signal input terminal SEL is connected with the output of the control signal generator 12, and the alternating signals outputted from the control signal generator 12 are used as the selecting signal of the first multiplexor U3. When a LOW voltage signal is inputted into the selecting signal input terminal SEL, the inputted signals to the first set of signal input terminal X1 and Y1 are outputted from the signal output terminal X3 and Y3. When a HIGH voltage signal is inputted into the selecting signal input terminal SEL, the inputted signals to the second set of signal input terminal X2 and Y2 are outputted from the signal output terminal X3 and Y3. In other words, the LOW voltage and the HIGH voltage of the selecting signal input terminal

6

SEL will make the first USB interface 14 and the second USB interface 15 to be connected with the third USB interface 16 respectively.

Referring to Fig. 3, which is the circuit diagram of a second embodiment according to the present invention. As shown in the figure, wherein the control signal generator 12 comprises two D FLIP-FLOPs (or equivalent circuits). The clock signal input terminal CP of the first D FLIP-FLOP U2 is connected with the output of the trigger signal generator 11, while the reverse data output terminal QN is connected with its data input terminal D. The clock signal input terminal CP of the second D FLIP-FLOP U4 is connected with the reverse data output terminal QN of the first D FLIP-FLOP U2, while the reverse data output terminal QN of the second D FLIP-FLOP U4 is connected with its data input terminal D, and the positive data output terminals Q of the first D FLIP-FLOP U2 and the second D FLIP-FLOP U4 are used as the control signals for the connector 13. When the clock signal input terminal CP of the first D FLIP-FLOP U2 receives a pulse signal, the voltage of its data input terminal D will be moved the positive data output terminal Q, while a reverse voltage of the original data input terminal D will be formed at the reverse data output terminal QN, and the voltage of the reverse data output terminal QN will then be sent back to the data input terminal D. When the next pulse signal is inputted to the control signal generator 12, the voltage of the data input terminal D will be moved to the positive data output terminal Q of the first D FLIP-FLOP U2, and now the voltage of the positive data output terminal Q is opposite to the voltage generated by the previous pulse signal inputted to the

control signal generator 12. Thus a HIGH voltage and a LOW voltage will be generated alternately. The voltage of the reverse data output terminal QN of the first D FLIP-FLOP U2 is used as a trigger signal to be inputted to the clock signal output terminal CP of the second D FLIP-FLOP U4, thus the positive data output terminal Q of the second D FLIP-FLOP U4 also generates HIGH and LOW voltages alternately, having a frequency just a half of the first D FLIP-FLOP U2's. Therefore, four patterns of LOW and LOW voltages, HIGH and LOW voltages, LOW and HIGH voltages, HIGH and HIGH voltages are obtained at the positive data output terminals Q of the first D FLIP-FLOP U2 and the second D FLIP-FLOP U4, and are outputted alternately as the control signals to let the connector 13 connect different USB interfaces.

Referring to Fig. 4, which is the circuit diagram of a third embodiment according to the present invention. The difference between the circuit in Fig. 4 and the aforementioned electronic switching device for USB interface is the internal resistance in the connector 13. As shown in the figure, a first multiplexor U3 and a second multuplexor U3'are parallelly connected in the connector 13, so as to decerase the internal resistance in connector 13, therefore, the quality of the signal transmmision between USB interfaces are enhanced, and the distance between USB interfaces can be increased.

Referring to Figs. 5 and 6, which are the schematic block diagram and the circuit diagram of the first embodiment of the present invention showing that a delay signal generator 17 is added. As shown in the figures, the delay signal generator 17 comprises a resistor R2, a capacitor C2 and a diode D1 (see Fig. 6), having its

8

input to be connected with the output of the trigger signal generator 11, and its output to be connected with the enable terminal OE of the connector 13. The resistor R2 and the capacitor C2 are serially connected between VCC and GND, one end of the resistor R2 is connected with VCC, while the other end thereof is connected with one end of the capacitor C2, having a voltage V2, the other end of the capacitor C2 is connected to GND, the positive terminal of the diode D1 is connected with the voltage V2, while the negative terminal thereof is connected with one end of the resistor R3, the other end of the resistor R3 is the input terminal for the delay signal generator 17, and V1 (the output of the trigger signal generator 11) is used as the input of the delay signal generator 17, V2 is the output of the delay signal generator 17.

When the switch SW1 of the trigger signal generator 11 is conducting, the voltage V1 will be changed from HIGH voltage to LOW voltage, so the voltage V2 will also be changed from HIGH voltage to LOW voltage. When the switch SW1 of the trigger signal generator 11 is opened, the voltage V1 will be changed from LOW voltage to HIGH voltage, so the voltage V2 will also be changed from LOW voltage to HIGH voltage. In order to delay the time of V2 from LOW voltage to HIGH voltage, the present invention selects a capacitor having a longer time constant as the second capacitor C2. When the switch SW1 of the trigger signal generator 11 is conducting, the enable terminal OE of the connector 13 will be LOW voltage, thus the USB interfaces are all disconnected. After a while, the voltage V2 will be changed from LOW voltage to HIGH voltage, and the related USB interfaces are connected according to the control

signals outputted from the control signal generator 12. The design of the present invention is to let the user turn the switch sequentially to select the required USB interface connection (e.g. push the switch button once to select the first device, and push the switch button twice to select the second device). However, if a user pushes the switch several times quickly, the unrelated intermediate USB interfaces might be conducting to cause signal confusing and disable the whole system, therefore, a delay signal generator 17 is needed to avoid unrelated device to react due to the delay saturation of the voltage V2.

Referring to Figs. 7 and 8, which are the schematic circuit block diagram and the circuit diagram of the first embodiment of the present invention showing that a display 18 is added. As shown in the figures, the input of the display 18 is connected with the output of the control signal generator 12, the different signals outputted from the control signal generator 12 will make LED 1, LED 2 conducting respectively, so as to show the connections between different USB interfaces.

Referring to Figs. 9 and 10, which are the schematic circuit block diagram and the circuit diagram of the first embodiment of the present invention showing that an enable signal generator 19 is added. As shown in the figure, the output of the enable signal generator 19 is connected with the control signal generator 12. The enable signal generator comprises a resistor R4 and a capacitor C4, wherein the resistor R4 and the capacitor C4 are serially connected between VCC and GND. One end of the resistor R4 is connected to GND, while the other end thereof is connected with one end of the capacitor C4,

10

having a voltage V3. The other end of the capacitor C4 is connected with VCC. When VCC is conducting, V3 will be changed from LOW voltage to HIGH voltage immediately, and sent to the reset terminal R of the first D FLIP FLOP U2 of the control signal generator 12 to clear the output of the first D FLIP FLOP U2 to LOW voltage. After a while, since the capacitor C4 is charged, V3 will be changed from HIGH voltage to LOW voltage, and maintained at LOW voltage, and the control signal generator 12 will not be influenced by the enable signal generator 19. Thus the connections between different USB interfaces are the same whenever the VCC begins conducting.

Furthermore, VCC will be used as the HIGH voltage of the present invention, no other power supply is needed, and a diode can be connected between VCC and each USB interface to avoid the reverse current flowing from USB interface to VCC.

In addition, the pulse signal outputted from the trigger signal generator 11 can be a positive or a negative pulse signal, and the number of the control signal outputted from the control signal generator is not limited. The numbers of the display, multiplexors and USB interfaces are also not limited.

The above embodiments are only used for description, and can not be treated as a limitation. The spirit and scope of the present invention will only be limited by the appended claims.

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